REMARKS

The Office Action mailed June 15, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

No extension of time is believed to be required based upon the filing of this Amendment prior to the deadline of the three-month statutory period (i.e., September 15, 2004). Authorization is granted to charge counsel's Deposit Account No. 01-2300, referencing **Attorney Docket No. 108397-00106**, for any additional fees necessary for entry of this Amendment.

Claims 52, 55 and 56 have been amended. Applicant submits that the amendments made herein are fully supported in the Specification and the drawings, as originally filed, and therefore no new matter has been introduced. Specifically, support for the amendments can be found in Fig. 9 of the present application. Accordingly, claims 44-56 are pending in the present application and are respectfully submitted for reconsideration.

Claims 44-54 and 56 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the Brant et al. patent (U.S. Patent No. 5,799,200). Dependent claims 45-47, 49-51 and 53-54 depend from independent claims 44, 48, 52, respectively. Claim 52 has been amended. The rejections are respectfully traversed and reconsideration is requested.

Independent claim 44 recites a method of operating a semiconductor memory including dynamic memory cells, comprising the step of entering a low power consumption mode, in which the dynamic memory cells do not retain data therein by prohibiting refresh operations, in response to a dedicated external control signal.

Independent claim 48 recites a method of controlling a semiconductor memory including dynamic memory cells, comprising the step of outputting a dedicated control signal to the semiconductor memory so that the semiconductor memory enters a low power consumption mode, in which the dynamic memory cells do not retain data therein by prohibiting refresh operations.

Independent claim 52, as amended, recites a memory system comprising a first memory including dynamic memory cells, having a low power consumption mode in which the dynamic memory cells do not retain data therein while power is on by prohibiting refresh operations, and the first memory having a data terminal; and a second memory including flash memory cells, having a data terminal which is connected with the data terminal of the first memory.

Independent claim 56, as amended, recites a method of controlling a first memory including dynamic memory cells, having a low power consumption mode in which the dynamic memory cells do not retain data therein while power is on by prohibiting refresh operations, and a second memory including flash memory cells, comprising the steps of transferring data stored in the dynamic memory cells in the first memory to the flash memory cells in the second memory before the first memory enters the low power consumption mode; and transferring data stored in the flash memory cells in the second memory to the dynamic memory cells in the first memory after the first memory exits the low power consumption mode.

The Brant et al. patent is directed to a data processing system having the operational advantages of volatile memory devices with relatively large memory capacity and the further advantages of non-volatile retention of data in response to power failures. A single module containing both a DRAM and a Flash ROM works to automatically preserve data in the event

electrical power is lost from a primary power source. Data is moved from the DRAM to the Flash ROM where it remains as long as power is not available from the primary source.

Applicant respectfully submits that the Brant et al. patent does not disclose or suggest the memory system and methods, as claimed in the present invention. Specifically, with respect to claims 44-51, the Brant et al. patent fails to disclose a way to enter or exit a semiconductor memory to or from a low power consumption mode in response to a dedicated external control signal. Therefore, as a result, the Brant et al. patent cannot achieve the effect of having DRAM reliably enter low power consumption mode and be released from the mode by a dedicated low power consumption mode signal/LP. (Specification, p. 32, ls. 15-17) In addition, with respect to claims 52-54 and 56, as amended, the Brant et al. patent fails to disclose a low power consumption mode that prohibits refresh operations when the power is on. Moreover, because the memory system of the claimed invention can enter low power consumption mode while keeping the power of the DRAM on, the DRAM and the flash memory can have a common power supply.

In contrast, in the Brant et al. patent, because the flash memory needs to keep its power on while the DRAM has its power off, the flash memory and the DRAM need to each have individual power supplies. In other words, the control circuit for the memory system in the Brant et al. patent needs to control the on and off of each of the DRAM's and the flash memory's power supplies separately. Further, with respect to dependent claims 53 and 54, the Brant et al. patent fails to disclose the operations as claimed. The operations of claims 53 and 54 each correspond to the operations in Figs. 9(b) and 9(a) of the present invention, respectively. These operations are not disclosed in the Brant et al. patent because they are performed during the period when the power is on, a period not disclosed in the Brant et al. patent. For example, in the

present invention, after DRAM enters an idle mode, the data retained in flash memory are transferred to DRAM. (Fig. 9(a)) During the service state, DRAM is used as the work memory. When the service state shifts to a waiting state, the data of the DRAM necessary to be retained are saved in flash memory. (Fig. 9(b)) Accordingly, the Brant et al. patent does not disclose or suggest the memory system and methods, as claimed.

Based upon the forgoing, Applicant respectfully submits that each and every element recited within independent claims 44, 48, 52 and 56 is neither disclosed nor suggested by the Brant et al. patent, and therefore these claims are patentable and in condition for allowance. Reconsideration is requested.

It is further submitted that dependent claims 45-47, 49-51 and 53-54 are also patentable and in condition for allowance due to their dependency upon independent claims 44, 48 and 52, respectively, since the dependent claims differ in scope from the corresponding parent claims. Dependent claims 45-47, 49-51 and 53-54 depend from independent claims 44, 48 and 52, respectively, and thus are further limited to additional features of the invention. Therefore, it is respectfully submitted that the dependent claims 45-47, 49-51 and 53-54 are patentable over the Brant et al. patent for at least the reasons set forth above with respect to independent claims 44, 48 and 52. Reconsideration is requested.

Independent claim 55 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the Brant et al. patent in view of the Jha et al. patent (U.S. Patent No. 6,407,949). The rejection is respectfully traversed and reconsideration is requested.

Independent claim 55, as amended, recites a cellular phone having a service state and a waiting state, comprising a first memory including dynamic memory cells, having a low power consumption mode in which the dynamic memory cells do not retain data therein while power is

on by prohibiting refresh operations, and the first memory having a data terminal; and a second memory including flash memory cells, having a data terminal which is connected with the data terminal of the first memory, wherein data stored in the dynamic memory cells in the first memory is transferred to the flash memory cells in the second memory then the first memory enters the low power consumption mode upon shifting from the service state to the waiting state, and wherein the first memory exits the low power consumption mode then data stored in the flash memory cells in the second memory is transferred to the dynamic memory cells in the first memory upon shifting from the waiting state to the service state.

The Jha et al. patent is directed to mobile communication devices having integrated embedded flash and static random access memory (SRAM). The flash and SRAM memory are embedded within an application specific integrated circuit (ASIC) to provide improved access times and also reduce overall power consumption of a mobile telephone employing the ASIC. Applicant respectfully submits that neither the Brant et al. patent nor the Jha et al. patent, alone or in alleged combination, does not disclose or suggest the cellular phone having a service state and a waiting state, as claimed in the present invention.

As acknowledged by the Examiner, the Brant et al. patent "does not explicitly disclose that a processing system [sic] having the above features are used in a cellular phone having a service state (on state) and a waiting state (off state)." The Examiner proceeds to rely on the Jha et al. patent as disclosing "a mobile communication device such as cellular telephones having integrated embedded non-volatile (flash memory), which retain data after power is disconnected [sic], and a volatile memory, which have large memory capacity and high operational speed (col. 1, line 13-46)." The Jha et al. patent, however, appears to merely disclose that power consumption can be reduced by embedding flash memory and SRAM within an ASIC. Indeed,

the same arguments set forth above distinguishing the present invention from the Brant et al. patent are also applicable to distinguishing the present invention from the Jha et al. patent. Specifically, the Jha et al. patent fails to disclose, in pertinent part, dynamic memory cells, having a low power consumption mode in which the dynamic memory cells do not retain data therein while power is on by prohibiting refresh operations. The Jha et al. patent further fails to disclose that data stored in dynamic memory cells is transferred to flash memory cells when DRAM enters low power consumption mode upon shifting from a service state to a waiting state, and the data is transferred from flash memory cells to DRAM when DRAM exits lower power consumption mode upon shifting from a waiting state to a service state. (Figs. 9(a) and 9(b)) Accordingly, the Jha et al. patent also does not disclose or suggest the cellular phone, as claimed.

Since neither the Brant et al. patent nor the Jha et al. patent discloses the cellular phone, as claimed in the present invention, it is submitted that the alleged combination of these references also does not disclose or suggest the claimed invention. Nor even if the references were combinable, as suggested, would such alleged combination result in the claimed invention. It is therefore submitted that the references, either alone or in alleged combination, fail to disclose or suggest the cellular phone of the present invention. Based upon the forgoing, it is respectfully submitted that independent claim 55 is patentable and in condition for allowance. Reconsideration is respectfully requested.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned

counsel at the telephone number, indicated below, to arrange for an interview to expedite the disposition of this application.

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Respectfully submitted,

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